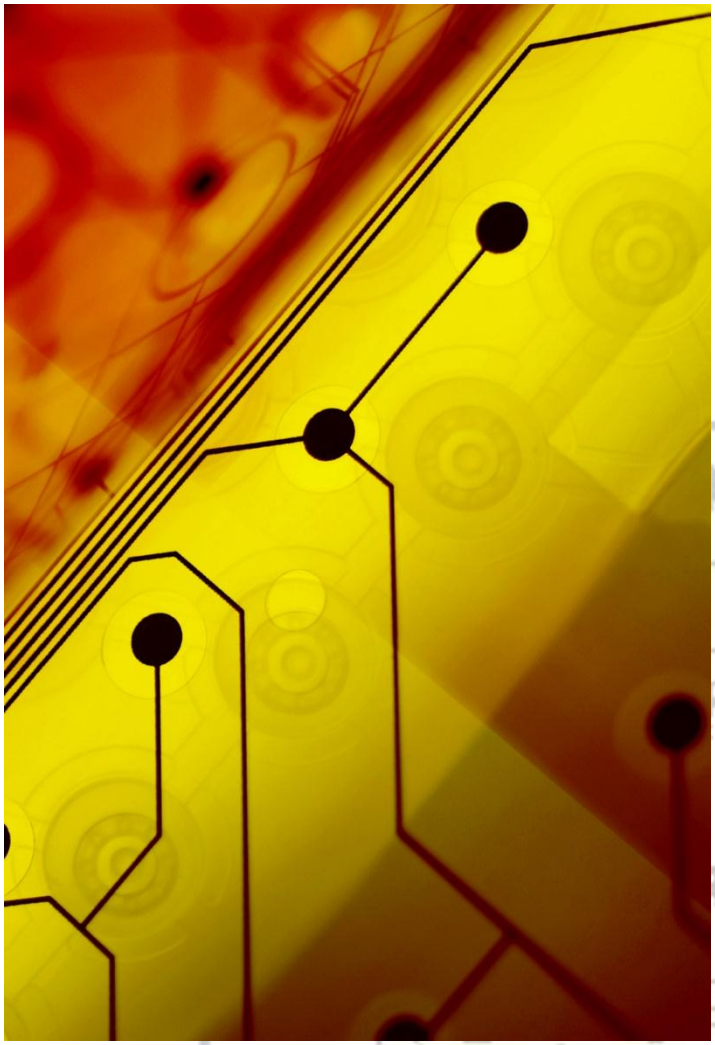

# [Question Bank]

**LAB:**

**DIGITAL SYSTEM DESIGN**

**Code: ECE-354**

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**Subject Teacher:**

**Dr. Harjinder Singh**

**Semester V$^{th}$**

**This booklet Includes:**

- List of Equipments
- List of Softwares
- List of Experiments
- lab Manual
- Question Bank

## ECE 354 DIGITAL SYSTEM DESIGN LAB

### QUIZ QUESTIONS

### CHAPTER- COMBINATIONAL CIRCUITS

1. Design a two bit magnitude comparator to compare equality.
2. Explain Arithmetic logic unit (ALU).
3. Design hexadecimal to binary encoder for 4- bits.
4. Design binary to decimal decoder for 4- bits.
5. Design a 4- bit Binary to Grey code converter.
6. Design a 4-bit Gray code to Binary code convertor.
7. Explain in brief multiplication and division of unsigned binary integers.
8. Design the $4 \times 16$ decoder with $2 \times 4$ decoder.
9. Implement half adder circuit using 4:1 MUX or multiplexers only.
10. Implement using 4:1 MUX.

    $F = \in m\ (0, 3, 4, 7)$

11. Design full adder using logic gates.
12. Implement the Boolean function with three half adder circuit F=ABC.
13. Implement the following function using a 3 line to 8 line decoder

    $S\ (A, B, C) = \in m\ (1, 2, 4, 7)$

    $C\ (A, B, C) = \in m\ (3, 5, 6, 7)$

14. Implement the following Boolean function with a multiplexer

    $F\ (A, B, C, D) = \in m\ (0, 1, 3, 4, 8, 9, 15)$

15. Design a combinational circuit which has four inputs and one output. The output is equal to 1 when:
    1. All the inputs equal to 1 or
    2. None of the inputs equal to 1
    3. An odd number of inputs are equal to 1.

Draw the logic circuit with minimum number of NAND gates.

16. Implement the following function using 4:1 MUX

    F = ∈m (0, 3, 4, 5, 6, 7)

17. Implement the following logic function using 8:1 MUX

    F = ∈m (0, 1, 2, 3, 4, 10, 11, 14,15)

18. Design and implement a 4-bit Gray code to binary code convertor using 4 to 16 decoder IC.

19. Draw the logic circuit for the following expression

    $$F = \bar{A}B + A\bar{B}\bar{C}$$

20. Draw the logic circuit for the following expression

    $$F = \bar{x}\bar{y}z + \bar{x}yz + x\bar{y}$$

21. Implement the following function using 3 to 8 decoder

    F (A, B, C) = ∈m (0, 1, 3, 4, 5, 7)

22. Implement the Boolean function with three half adder circuit

    $$F = A'BC + AB'C$$

23. Draw the gate implementation of the simple fixed Boolean function.

    F (A, B, C) = $A'C + A'A + AB'C + BC$ using AND and OR gates.

24. Design 4:1 MUX.

25. Design 8:1 MUX by using two 4:1 MUX.

26. Design a comparator circuit which compares two 2- bit numbers. It has three outputs $A > B$, $A < B$ and $A = B$. Also show that $A < B = \overline{A > B}.\overline{A = B}$ .

27. Design a combinational circuit with 3 inputs and 1 output. The output is high only when more than one input is high.

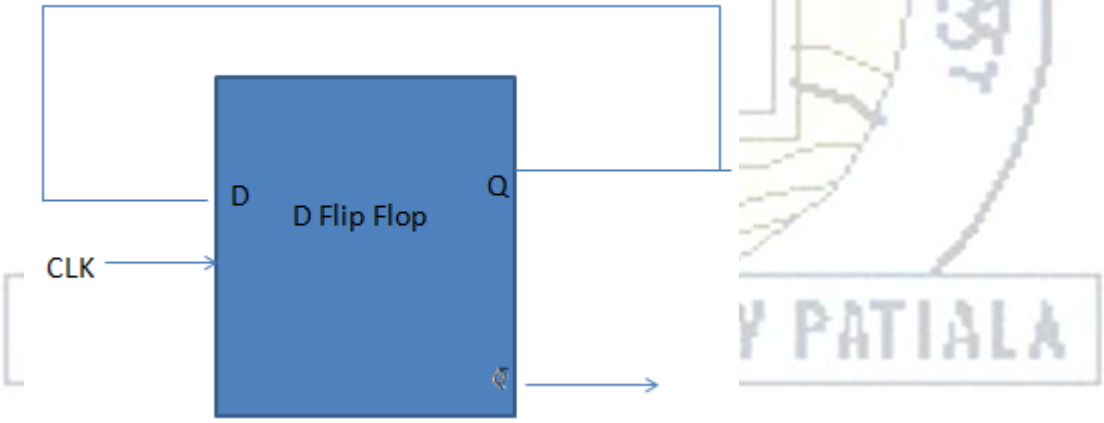
28. Design a circuit that generate an even parity bit for 4- bit input and implement it using only NAND gates.
29. Design a BCD TO Gray Code Convertor.
30. Implement the following function using $8 * 1$ and $16 * 1$ multiplexer.

    F (a, b, c, d) = $\in$m (0, 1, 2, 3, 4, 5, 8, 9, 10, 11, 15)

31. Design full subtractor using one 3:8 decoder.

CHAPTER- SEQUENTIAL CIRCUITS

32. Design the following sequence generator using D flip- flop.
33. Draw the output waveforms for the following input signals (CLK, S and R).
34. Draw the waveform at output ($\overline{Q}$) for 5 clock pulses, Assume Q=1 as initial condition for the given circuit:




35. Design the following sequence generator using D flip-flops


36. Draw a logic symbol for a D- flip flop and compare with RS flip-flop.
37. Give the truth table for each flip flop type: (1) J-K, (2) d, (3) T.

CHAPTER- COUNTERS AND REGISTERS

38. Design MOD-5 asynchronous counter ( or ripple counter).
39. Design MOD-5 asynchronous counter using JK flip flop and a NAND gate.
40. Design JK counter that goes through states 0, 2, 3, 5, 6 only.
41. Design a J-K flip flop counter that goes through the states 1, 3, 5, 7, 1, 3.... . Is the counter self-correcting?
42. Design an up- down 3-bit synchronous counter using JK flip flop to count the following sequence 0, 2, 3, 6, 4, 0.
43. Design a synchronous J-K counter that goes through states 1, 2, 4, 7, 1, 2, ..... .
44. Design a synchronous J-K counter that goes through the following states 1, 3, 4, 5, 7, 1, 3, .... .
45. Design a synchronous JK counter that goes through the following states 2, 4, 7, 2, 4..... . Is the counter self starting?
46. Design a synchronous JK counter that goes through the states- 1, 2, 3, 6.
47. Design a counter using T flip flop to count the following state diagram states.
48. Design a Up- down synchronous counter using D flip flop to count the following sequence: 0, 5, 7, 6, 3, 2, 4, 0.
49. Design a synchronous counter using T flip flop that goes from the following states: 0→5 →6 →3→ 7 →4 →1
50. Design a forward synchronous counter using T flip flop that goes through the following states:

    2, 4, 5, 6, 7, 2, 4, .....
51. Design J-K counter that goes through states: 0, 3, 5, 0.
52. Designing a synchronous counter using J-K flip- flops to count the following sequence: 1, 3, 5, 7, 1.....

53. Design a synchronous counter using T flip flops going through the following states only:

    0, 4, 6, 7, 9, 13, 15.

54. Design a synchronous 4-bit binary counter using T flip-flops.

55. Design a 4- bit synchronous counter using D flip flops to count the following sequence:

    0→3 →7 →5→ 4→13→0

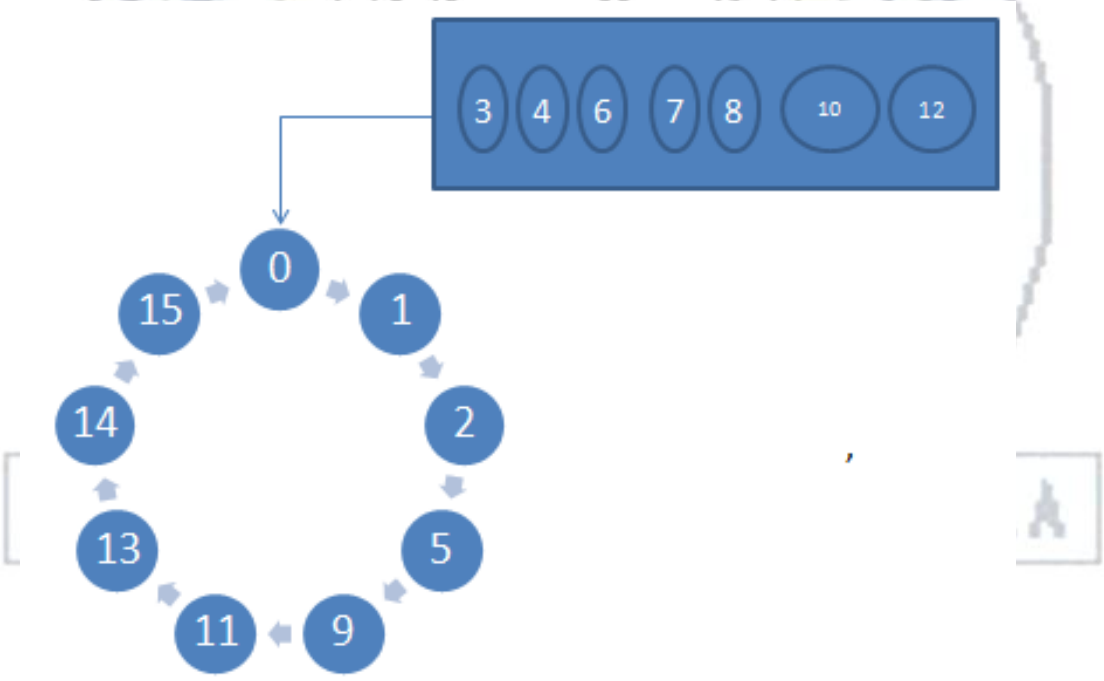
56. Design a synchronous counter using D flip flops to count the following states

    1→3 →5 →7→ 11→13→1

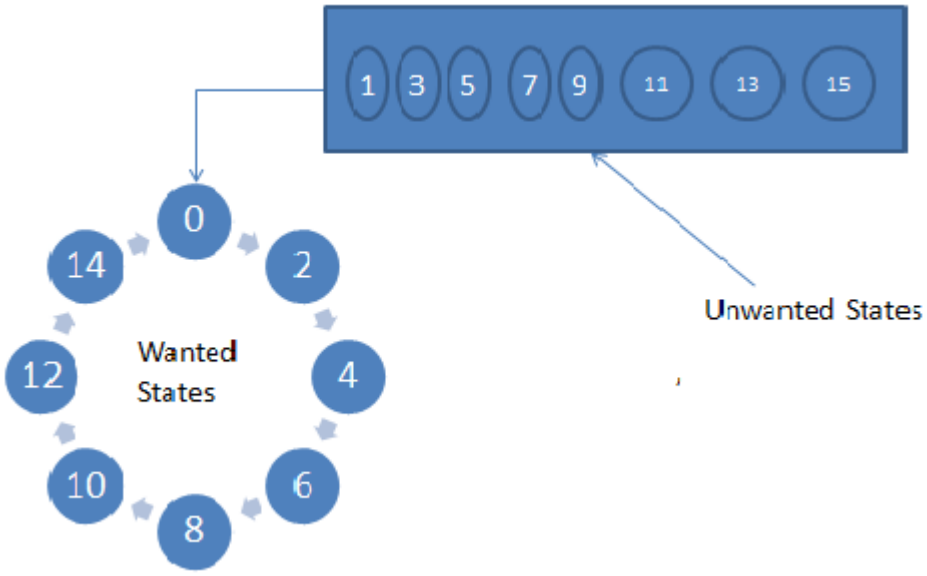
57. Design a 4- bit synchronous counter using JK flip flops to count the following states:

    0, 3, 5, 9, 11, 14.

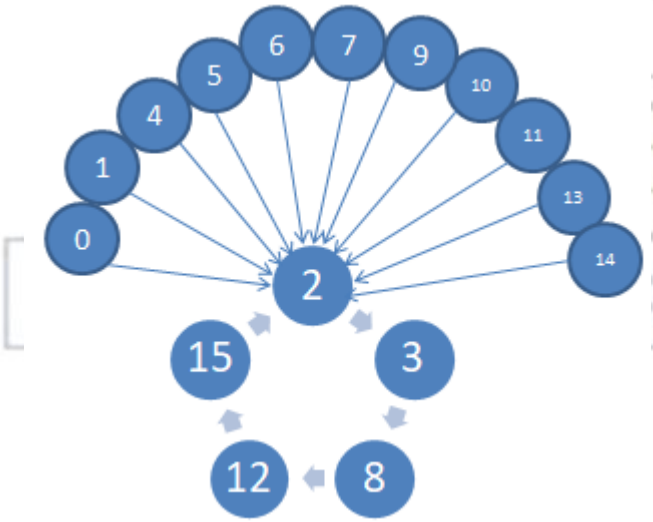
58. Design a 4- bit counter using D flip flop to count the following state diagram states



59. Design a synchronous counter to count the states of following state table

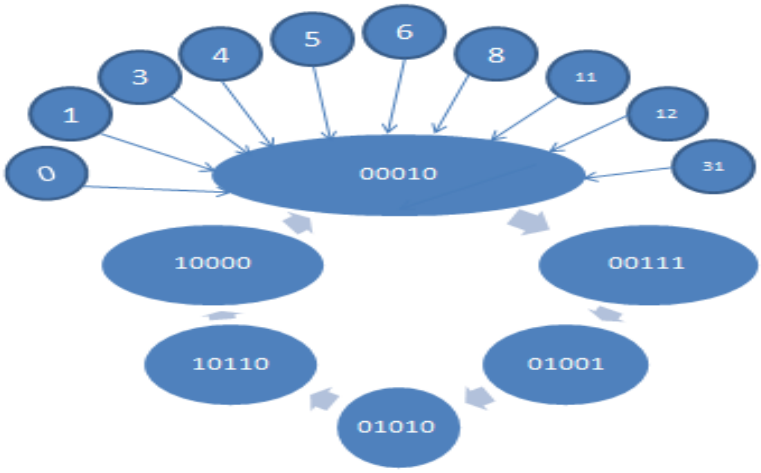



60. Design a synchronous J-K flip flop counter to count the following states 2, 3, 8, 12, 15, 2.....




61. Design a 5- bit synchronous counter using D flip- flops to count the following states 0, 2, 6, 8, 12, 16, 22, 28

62. Design a synchronous counter using T flip flops that counts the states as shown in state diagram



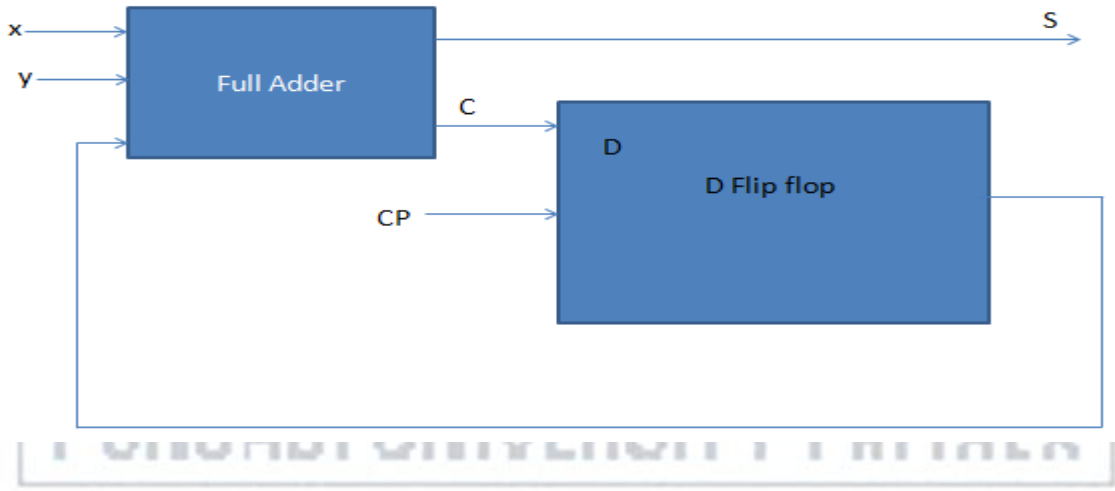

63. Design an up down counter using D flip flops to count 0, 3, 2, 6, 4, 0,.....
64. What is the basic difference between a counter and a shift register?
65. Design and draw the circuit of shift register to generate the following wave train .....1101011.....
66. Design a T- flip flop counter that goes through the states 2, 4, 5, 6, 7, 2, 4..... is the counter self correcting.
67. Design a synchronous decade counter to count in the following sequence 1, 0, 2, 3, 4, 8, 7, 6, 5.
68. Design a mod 30 synchronous up counter.
69. Design an up- down counter using JK flip flop to count 0, 2, 3, 6, 4, 0.....
70. Design 3- bit Binary counter using T flip flop.
71. Design MOD-5 Up- down counter using RD flip flops.
72. Design a MOD 6 counter using T- flip flop.
73. Design a three bit, MOD6, unit distance up- down counter.
74. Design mode- 8 synchronous counter using T flip flops.
75. Explain two applications of Shift Register as counters.

CHAPTER- SEQUENTIAL CIRCUITS

76. Determine the reduced state table for the following state table.

| Present State | Next States | | Output | |
|---|---|---|---|---|
| | X=0 | X=1 | X=0 | X=1 |
| 1 | 1 | 2 | 0 | 0 |
| 2 | 2 | 3 | 0 | 1 |
| 3 | 3 | 4 | 1 | 1 |
| 4 | 1 | 2 | 0 | 0 |
| 5 | 5 | 2 | 1 | 0 |

77. Derive the state table and state diagram of following sequential circuit




78. A sequential circuit has two JK flip flop A and B, two inputs X and Y and one output Z.

The flip- flop input equations and output functions are as follows:

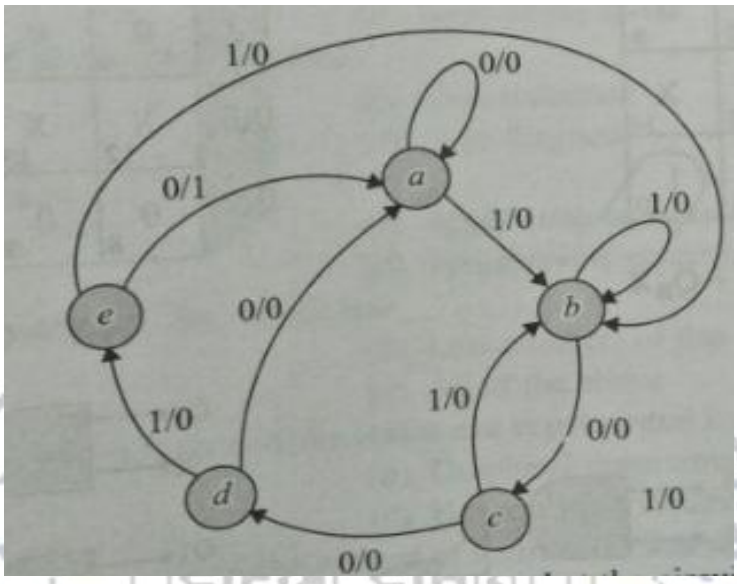
$$J_A = BX + \overline{B}\overline{Y},\ K_A = \overline{B}X\overline{Y}, Z = AXY + B\overline{X}\overline{Y}, J_B = \overline{A}X \text{ and } K_B = A + X\overline{Y}$$

79. Derive the sequential circuit with two D flip flops A and B and one input x.

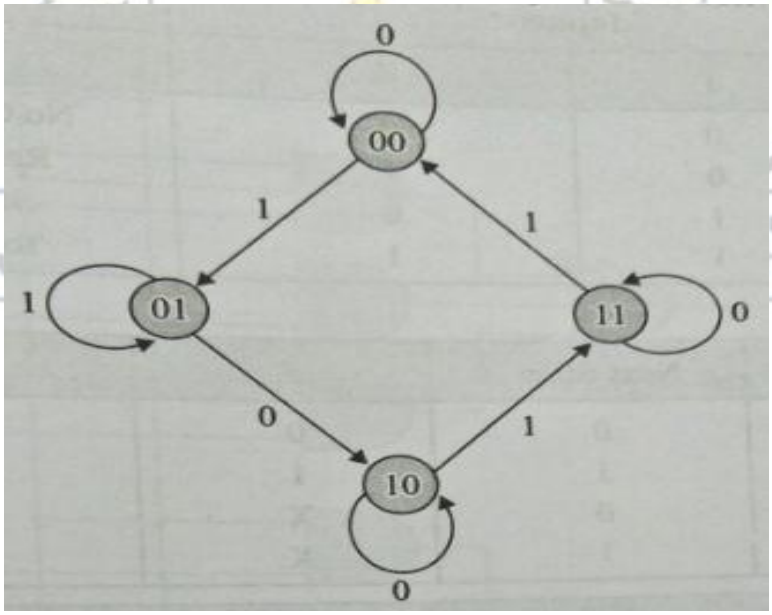
a. When x=1, the state of the circuit remains same.

b. When x=0, then circuit through the state transitions from 00 to 01 to 11 to 10 and back to 00 and repeats.

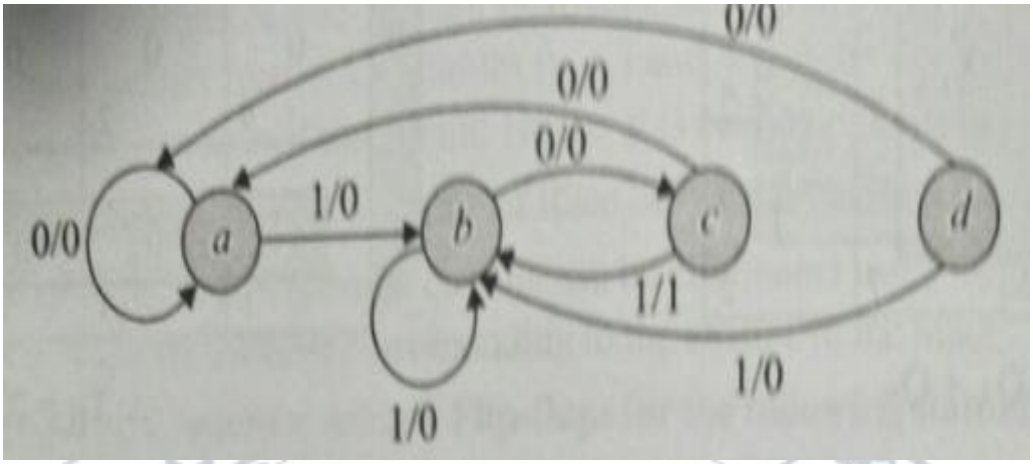
80. Reduce the following state diagram and design a circuit using D flip flop when (a= 001, b= 010, c=011, d=100, e=101).



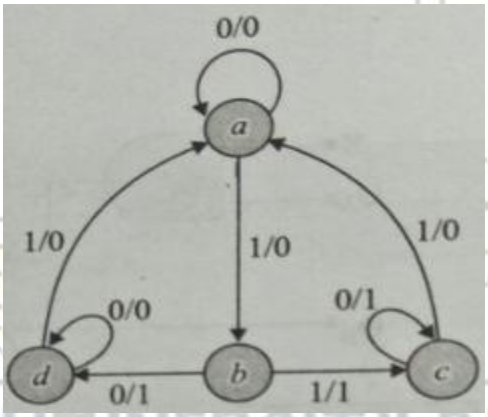

81. Design with D flip flop and JK flip flop the clocked sequential circuit whose state diagram is given in the following figure:



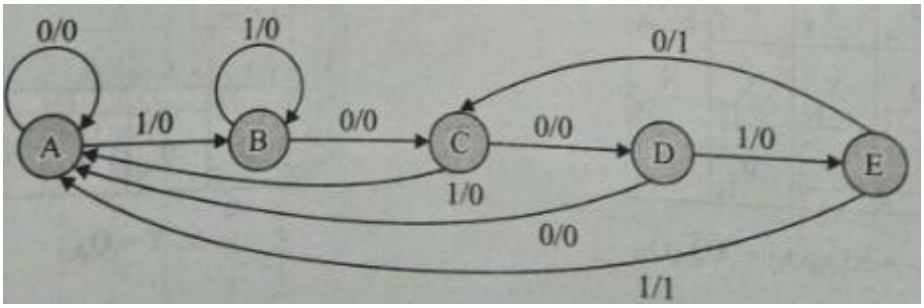
82. Design a clocked sequential machine using JK flip flops for the state diagram shown below. Use state reduction if possible. Make proper state assignment.



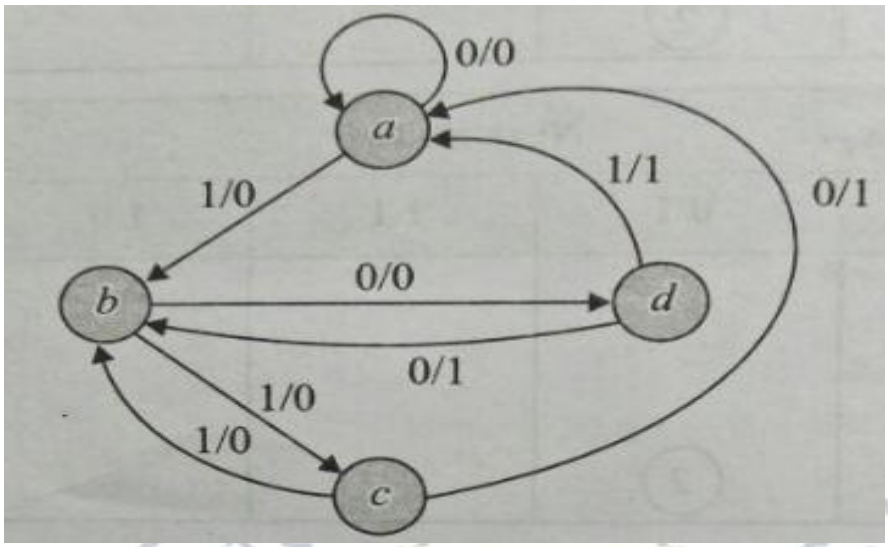

83. Design a circuit that will function according to state diagram given below




84. Design the sequential circuit using D flip flops for the state diagram as shown



85. Design a clocked sequential machine using T flip flops for the following state diagram. Use state reduction if possible. Also use straight binary state assignment.




86. Design the sequence detector for the given state diagram using T flip flops.